IN THE SPECIFICATION:

Please replace paragraph [0031] with the following amended paragraph:

[0031] A silicon substrate may be introduced into the integrated processing system 100 via a load lock ~~102~~ 106 or 104 and placed in RTP chamber 116, where a silicon oxide film may be formed on the silicon substrate, as shown in steps 200 and 202 of Figure 4. The structure, including the substrate and the silicon oxide film, may then be transferred to thermal processing chamber 110, where it is heated in an atmosphere comprising NH_3 to incorporate nitrogen into the silicon oxide film, as shown in steps 204 and 206. The structure may then be transferred to cool down chamber 108 and cooled, for example, to less than about 100°C in about 1 to about 2 minutes, as shown in step 208. The structure may then be transferred to plasma processing chamber 114, where it is exposed to a plasma comprising a nitrogen source to incorporate more nitrogen into the silicon oxide film and form the SiO_xN_y gate dielectric, as shown in steps 210 and 212. Optionally, the structure may be transferred to RTP chamber 116 where the structure may be annealed, as shown in steps 214 and 216. The structure may then be transferred to CVD processing chamber 118, as shown in step 218, and a gate electrode, such as a polysilicon layer or an amorphous silicon layer may be deposited on the structure, as shown in step 220. The structure may then be removed from the integrated processing system 100 via a load lock ~~102~~ 106 or 104.

Please replace paragraph [0033] with the following amended paragraph:

[0033] A silicon substrate may be introduced into the integrated processing system 300 via a load lock ~~302~~ 306 or 304 and placed in RTP chamber 316, where a silicon oxide film may be formed on the silicon substrate. The structure, including the substrate and the silicon oxide film, may then be transferred to thermal processing chamber 310, where it is heated in an atmosphere comprising NH_3 to incorporate nitrogen into the silicon oxide film. The structure may then be transferred to cool down

chamber 308 and cooled, for example, to less than about 100°C in about 1 to about 2 minutes. The structure may then be transferred to plasma processing chamber 314, where it is exposed to a plasma comprising a nitrogen source to incorporate more nitrogen into the silicon oxide film and form the SiO_xN_y gate dielectric. Optionally, the structure may then be transferred to RTP chamber 318 where the structure may be annealed. After the structure is annealed, the structure may be transferred out of the integrated processing system 300 via load lock ~~302~~ 306 or 304 to a processing chamber (not shown) external to the integrated processing system such as a low pressure chemical vapor deposition chamber (LPCVD), for depositing a gate electrode, such as a polysilicon layer or an amorphous silicon layer.